CONTACT

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Constantine, Algeria

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SKILLS

IC Design & Simulation

Analog/Mixed-Signal IC Design, Cadence Virtuoso, Spectre, MATLAB/Simulink, Verilog-AMS / VHDL-AMS, XSCHEM, KLayout, Magic, NGSpice, Xyce

Hardware & PCB

LTSpice, KiCAD, Proteus, ngspice, Electronics, Digital/Analog Circuit Design, Signal Integrity, Oscilloscopes, Spectrum Analyzers, Function Generators, Soldering

Scripting & Tools

Linux/Bash, Git, Makefiles, LabVIEW, Python, Ruby, TCL

Firmware & HDL

Verilog / SystemVerilog, VHDL, FPGA

Programming Languages & Embedded

Python, Ruby, JavaScript, TypeScript, C#, C/C++, Assembly, Embedded Systems

Frameworks & Libraries

React.js, Next.js, Nest.js, Node.js, Blazor, ASP.NET Core, Entity Framework

Databases

MSSQL, MySQL, MongoDB, Redis

Automation & DevOps

PowerShell, C# Automation, VM Provisioning, Windows Server Administration, Dynamic DNS, CI/CD

LANGUAGES

Arabic
Native

English
Conversational

French
Conversational

Yacine Sotehi

Phd Student Analog/Mixed IC design

SUMMARY

Analog/Mixed-Signal IC Design Researcher with a Master's in Electronics Instrumentation and industry experience building full-stack Laboratory Information Systems (.NET/SQL). Currently pursuing a PhD, where I led the analog team for my first successful tapeout using the open-source IHP-SG13G2 PDK—designing a readout SoC for PT100 sensors, including the conditioning chain, digital calibration, POR, Ramp ADC, and PMU. Beyond chip design, I bridge the gap between hardware and software through CAD/EDA automation. I significantly improved the IHP PDK's KLayout PCells by automating contact/guard-ring placement, via-stacks, and density checks, and created dynamic, user-friendly PCells for current mirrors and differential pairs. I also developed a macro to connect the PDN to analog blocks. These contributions were accepted via pull requests to the official IHP repository. I am seeking a role that leverages my IC design expertise while allowing me to apply my automation and software development skills to build better tools and workflows for chip design.

EXPERIENCE

Full-Stack Developer & IT Systems Engineer Sep 2023 – May 2025

BMLab · Algiers, Algeria

- Full-Stack Development: Built a Next.js/React ticketing system for the support team; optimized API performance and pagination.
- WASM Update Infrastructure: Designed a platform for auto-updating Blazor WebAssembly apps with partial updates to reduce bandwidth and downtime.
- Infrastructure Automation: Wrote C# and PowerShell scripts to automate VM provisioning/removal, software updates, dynamic DNS updates, and Windows Server 2022 migrations.
- Core Product Maintenance: Extended the flagship .NET/MSSQL LIS with new pages, performance optimizations, and bug fixes.
- Optimized API performance by replacing slow in-memory filtering (causing timeouts/OOM errors) with SQL-compiled LINQ predicates, server-side pagination, strategic indexes, and calculated fields—reducing load times from minutes to sub-second responses

EDUCATION

PhD Analog/Mixed IC design 2025 – Present

University of Blida 1 · Blida, Algeria

- Research Focus: Analog/Mixed-Signal IC Design, GM-C Filters
- First tapeout: IHP-SG13G2 (130nm), with contributions to conditioning chain, digital calibration, POR, and PMU.

Master Instrumentation 2021 – 2023

University of Constantine 1 · Constantine, Algeria · GPA 16/20

- Thesis: Digital Oscilloscope with Wi-Fi Remote Access (±150V, 20 kHz, auto-calibration, ESP32 web interface).

B.Sc. Electronics 2018 – 2021

University of Constantine 1 · Constantine, Algeria

- Thesis: Sun Tracker

PROJECTS

SoC Readout IC

IHP-SG13G2 · https://github.com/YacineSot/IHP__SoC2263

Designed an ultra-low-power SoC for precision agriculture, achieving ±2°C accuracy over -10°C to +50°C. Led the analog team and took ownership of:

- Conditioning Circuit with digital calibration for PT100 linearization
- Power Management Unit (PMU) with low-dropout regulators
- Power-on-Reset (POR) and Clock Generator for system startup
- Ramp ADC for temperature-to-digital conversion

Digital Oscilloscope

Designed a ±150V input range, 20 kHz digital oscilloscope with auto-calibration and polarity detection (absolute value + sign for negative voltages).

- Engineered the analog front-end with a multiplexed ADC (1 V reference, ~1 Msps) and a dedicated Power Management Unit (PMU) using voltage regulators for stable operation.
- Integrated ESP32 firmware to read ADC data and transmit it via integrated Wi-Fi to an onboard interactive web application.
- Built a full-stack remote-control interface (web app served from the ESP32) enabling users to trigger, adjust voltage/time scales, and view live waveforms remotely—ideal for distance-learning labs.